Report No.：HS1203280170A
RA No .：0101174-E
Version：A

LATCH UP TEST REPORT

Company ：RAIO Technology Inc.

Model Name ：RA8872

Date Code ：1122-N

Date Received ：MAR 28, 2012

Date Tested ：APR 03, 2012

TESTING LABORATORY IS ACCREDITED BY:

IEC/IECQ 17025 certificate of independent test laboratory approval

Certificate No.：T1091

ISO 9001 certificate is approved by TUV CERT certification body of TUV NORD Cert GmbH

WE HEREBY CERTIFY THAT:

The test(s) shown in the attachment were conducted according to the indicating procedures. We assume full responsibility for the accuracy and completeness of these tests and vouch for the qualifications of all personnel performing them.

	Name	Signature	Date
Test Engineer	Wallace Lee	Wallace Lee	Apr 03, 2012
Manager	Even Lin		Apr 03, 2012

NOTE：

1. This report will be invalid if reproduced in whole or in part.
2. This report refers only to the specimen(s) submitted to test, and is invalid if used separately.
3. This report is ONLY valid with the examination seal and signature of this institute.
4. The tested specimen(s) will only be preserved for thirty days from the date issued, if not collected by the applicant.

宜特科技股份有限公司 報告專用章 INTEGRATED SERVICE TECHNOLOGY

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1. GENERAL INFORMATION

1.1 DESCRIPTION OF UNIT

MANUFACTURER	: RAIO Technology Inc.
DEVICE NAME	: RA8872
DATE CODE	: 1122-N
PACKAGE / PIN COUNT	: LQFP-100
REFERENCE DOCUMENT	: JEDEC STANDARD NO.78 MARCH 1997
TRIGGER CURRENT	: +IT: 50mA ~ 200mA (+), Step: 50mA(+) Limit:1.5 x Vmax -IT: 50mA ~ 200mA (-), Step: 50mA(-) Limit:0.5 x Vmax
V SUPPLY OVER VOLTAGE TEST	: VCC3.3V: 3.3V ~ 5.5V (+) , Step: 0.1V (+) VCC1.8V: 1.8V ~ 3V (+) , Step: 0.1V (+)
MAXIMA RATED TEMPERATURE	: ROOM TEMPERATURE
SAMPLE QUANTITY	: 9 ea
FAILURE CRITERIA	: < 25mA 10mA + I normal > 25mA 1.4 x I normal
I NORMAL	: VCC3.3V: 12mA VCC1.8V: <1mA

2. LATCH UP TEST

2.1 TEST EQUIPMENT

Test Equipment	Equipment Number	Tester
KEYTEK ZAPMASTER	#MK2/1	10116

2.2 LABORATORY AMBIENCE CONDITION

Temperature：25°C±5°C

Relative humidity：55%±10% (RH)

2.3 REFERENCE DOCUMENT

The test is based on JEDEC STANDARD NO.78 MARCH 1997

2.4 TEST CONDITION

POSITIVE I

NEGATIVE I

Vsupply OVER VOLTAGE TEST

2.5 BIAS DESCRIPTION

VCC3.3V = 3.36 V(MAX)

VCC1.8V= 1.98 V(MAX)

VSS = 0V

2.6 SUMMARY OF TEST

Trigger Mode	Test Pin	Sample Quantity	Tested Result	I Trigger : Class I
I Trigger (+)	I/O3.3V	3	PASS(+200mA)	Class I Latch-up testing performed at room temperature. Class II Latch-up testing performed at maximum rated temperature.
	I/P3.3V		PASS(+200mA)	
	O/P3.3V		PASS(+200mA)	
I Trigger (−)	I/O3.3V	3	PASS(-200mA)	
	I/P3.3V		PASS(-200mA)	
	O/P3.3V		PASS(-200mA)	
Over Volt Test V_{supply}	VCC3.3V	3	PASS(+5.5V)	
	VCC1.8V		PASS(+3V)	

I/O3.3V:4,14,15,19-24,64-66,67-71
O/P3.3V:33,34,36,37,74,76,81-100
VCC1.8V:17,57
NC:5-8,26,28-30,39,43-49,52-56,58,60,62,63,67, 68,72,73,75,80
I/P3.3V:9-13,38,40-42
VCC3.3V:2,18,27,32,61,77,79
VSS:1,3,16,25,31,35,50,51,59,78

2.7 CONTENTS OF TEST

POSITIVE I (UNIT:mA)							
Test Pin TRIGGER CURRENT	#1	#2	#3	Test Pin TRIGGER CURRENT	#1	#2	#3
4	PASS	PASS	PASS	69	PASS	PASS	PASS
9	PASS	PASS	PASS	70	PASS	PASS	PASS
10	PASS	PASS	PASS	71	PASS	PASS	PASS
11	PASS	PASS	PASS	74	PASS	PASS	PASS
12	PASS	PASS	PASS	76	PASS	PASS	PASS
13	PASS	PASS	PASS	81	PASS	PASS	PASS
14	PASS	PASS	PASS	82	PASS	PASS	PASS
15	PASS	PASS	PASS	83	PASS	PASS	PASS
19	PASS	PASS	PASS	84	PASS	PASS	PASS
20	PASS	PASS	PASS	85	PASS	PASS	PASS
21	PASS	PASS	PASS	86	PASS	PASS	PASS
22	PASS	PASS	PASS	87	PASS	PASS	PASS
23	PASS	PASS	PASS	88	PASS	PASS	PASS
24	PASS	PASS	PASS	89	PASS	PASS	PASS
33	PASS	PASS	PASS	90	PASS	PASS	PASS
34	PASS	PASS	PASS	91	PASS	PASS	PASS
36	PASS	PASS	PASS	92	PASS	PASS	PASS
37	PASS	PASS	PASS	93	PASS	PASS	PASS
38	PASS	PASS	PASS	94	PASS	PASS	PASS
40	PASS	PASS	PASS	95	PASS	PASS	PASS
41	PASS	PASS	PASS	96	PASS	PASS	PASS
42	PASS	PASS	PASS	97	PASS	PASS	PASS
64	PASS	PASS	PASS	98	PASS	PASS	PASS
65	PASS	PASS	PASS	99	PASS	PASS	PASS
66	PASS	PASS	PASS	100	PASS	PASS	PASS

NEGATIVE I (UNIT:mA)							
Test Pin TRIGGER CURRENT	#1	#2	#3	Test Pin TRIGGER CURRENT	#1	#2	#3
4	PASS	PASS	PASS	69	PASS	PASS	PASS
9	PASS	PASS	PASS	70	PASS	PASS	PASS
10	PASS	PASS	PASS	71	PASS	PASS	PASS
11	PASS	PASS	PASS	74	PASS	PASS	PASS
12	PASS	PASS	PASS	76	PASS	PASS	PASS
13	PASS	PASS	PASS	81	PASS	PASS	PASS
14	PASS	PASS	PASS	82	PASS	PASS	PASS
15	PASS	PASS	PASS	83	PASS	PASS	PASS
19	PASS	PASS	PASS	84	PASS	PASS	PASS
20	PASS	PASS	PASS	85	PASS	PASS	PASS
21	PASS	PASS	PASS	86	PASS	PASS	PASS
22	PASS	PASS	PASS	87	PASS	PASS	PASS
23	PASS	PASS	PASS	88	PASS	PASS	PASS
24	PASS	PASS	PASS	89	PASS	PASS	PASS
33	PASS	PASS	PASS	90	PASS	PASS	PASS
34	PASS	PASS	PASS	91	PASS	PASS	PASS
36	PASS	PASS	PASS	92	PASS	PASS	PASS
37	PASS	PASS	PASS	93	PASS	PASS	PASS
38	PASS	PASS	PASS	94	PASS	PASS	PASS
40	PASS	PASS	PASS	95	PASS	PASS	PASS
41	PASS	PASS	PASS	96	PASS	PASS	PASS
42	PASS	PASS	PASS	97	PASS	PASS	PASS
64	PASS	PASS	PASS	98	PASS	PASS	PASS
65	PASS	PASS	PASS	99	PASS	PASS	PASS
66	PASS	PASS	PASS	100	PASS	PASS	PASS

V_{supply} OVERVOLTAGE TEST (UNIT: V)							
Test Pin TRIGGER VOLTAGE	#1	#2	#3	Test Pin TRIGGER VOLTAGE	#1	#2	#3
2	PASS	PASS	PASS	57	PASS	PASS	PASS
17	PASS	PASS	PASS	61	PASS	PASS	PASS
18	PASS	PASS	PASS	77	PASS	PASS	PASS
27	PASS	PASS	PASS	79	PASS	PASS	PASS
32	PASS	PASS	PASS				